REMARKS

Applicant respectfully requests consideration of the foregoing amendments submitted with the accompanying request for continued examination (RCE).

Upon entry of the attached amendments, claims 1-3, 5-7, 9, 10, 13-16, 22, and 23 have been amended. Claims 1-3, 5-7, 9, 10, 13-16, 22, and 23 are hereby amended to more particularly point out and distinctly claim the subject matter that Applicant regards as the invention. The subject matter in amended claims 1-3, 5-7, 9, 10, 13-16, 22, and 23 is included in the circuit embodiments illustrated in FIGs. 3A and 3B and described in the corresponding portion of the specification (page 8, line 27 to page 11, line 16). Consequently, no new matter is added.

Each objection and rejection presented in the Final Office Action mailed April 2, 2003 is discussed in the remarks that follow.

Reconsideration of the pending claims is respectfully requested, in view of the foregoing amendments and the following remarks.

I. Claim Objections

A. Statement of the Objection

Claims 3 and 13-23 are objected to because the phrases "propagated monotonically through said logic elements;" "propagate a plurality of signals monotonically;" and "during a launch cycle a set of signals monotonically to successive launch logic" are allegedly unclear.

B. Discussion of the Objection - Claims 3 and 13-23

Applicant respectfully traverses the objection of claims 3 and 13-23 for at least the reason that "monotonic progression" is a term-of-art used to describe digital-logic signal transfers within self-timed solid-state circuits. Such circuits use a transition-signaling protocol.

In a monotonic progression, only one direction of logic transition is considered. For example, in mousetrap logic gates, only the logic transition from a logic low to a logic high is considered, not the logic transition from a logic high to a logic low. As a result of the implementation of a monotonic progression, problems associated with static hazards are eliminated.

Self-timed solid-state circuits can be used to define vector logic states. Whereas, standard digital logic is binary, self-timed solid-state circuits can be used to encode more than two logic states.

The combination of an invalid logic state (which is ignored) and dynamic precharging allow one or more cascaded mousetrap logic gates to be "self-timed," or configured to operate asynchronously with respect to a clock source providing the precharge signals. In other words, clocks or other charging signals are used to merely precharge the mousetrap logic gates; the clocks do not dictate progression of the logic evaluation through the cascaded mousetrap logic gates. Triggering of each individual mousetrap logic gate is accomplished by a successful logic evaluation performed by the corresponding logic associated with the mousetrap logic gate. Hence, when using a vector logic system with mousetrap logic gates, two significant features can be determined from each vector output: (1) when the vector output is valid, thereby eliminating the need for a conventional valid clock signal, and (2) the value of the vector output when it is valid.

Applicant respectfully submits that the phrases objected to in the Office Action are clear to those skilled in the art of dynamic logic circuits. Nevertheless, Applicant has amended the claims to more particularly point out and distinctly claim the invention. Accordingly, Applicant respectfully requests that the objection of claims 3 and 13-23 be withdrawn.

II. Claim Rejections - Claims 1-23

A. Statement of the Rejection

Claims 1-23 presently stand rejected under 35 U.S.C. §102(b) as allegedly anticipated by Lesartre *et al.* (U.S. Patent No. 5,761,474 "the '474 patent.")

B. Discussion of the Rejection - Claims 1-23

1. Claims 1-9

Applicant respectfully traverses the rejection of claims 1-9 under 35 U.S.C. §102(b) for at least the reason that the cited reference fails to disclose, teach, or suggest each method step in the claims.

It is well established that "anticipation requires the disclosure in a single prior art reference of each element of the claim under consideration." *W.L. Gore &*

Associates, Inc. v. Garlock, Inc., 721 Fed 2d 1540, 220 U.S.P.Q. 303, 313 (Fed Cir 1983). The present rejection fails to meet the burden of identifying a single prior art reference that discloses, teaches, or suggests each feature of the claimed invention.

Applicant's claimed invention is fundamentally different than the system and method apparently disclosed in the '474 patent. As the title of the '474 patent indicates, it is directed to operand dependency tracking to determine when it is appropriate to execute an instruction in an out-of-order processor. In contrast, Applicant's claimed invention is directed to an instruction reordering mechanism that causes a plurality of logic elements to track which of the predefined plurality of said instructions are launched and causes the selection of no more than a predefined number of ports during a launch cycle. Identifying which instructions can be executed out-of-order based on operand dependencies, as apparently disclosed in the '474 patent, is not an instruction reordering mechanism that tracks which instructions are launched and causes the selection of no more than the predefined number of ports during the launch cycle.

For convenience of analysis, Applicant's independent claim 1, as amended, is repeated below in its entirety.

> 1. A method for finding a predefined plurality of instructions, if available, that are ready to be executed and that reside in an instruction reordering mechanism of a processor that can launch execution of instructions out of order via a predefined number of ports, comprising the steps of:
>
> (a) ***providing said instruction reordering mechanism*** having a plurality of said instructions, ***each said instruction port having a respective self-timed vector logic element for causing and preventing launching***, when appropriate, of said instruction; and
>
> (b) ***propagating a set of signals successively during a launch cycle through said self-timed vector logic elements of said instruction reordering mechanism.***

(Applicant's independent claim 1 - *emphasis added.*)

The cited art of record fails to disclose, teach, or suggest at least the emphasized steps of pending claim 1 as shown above. Consequently, claim 1 is allowable.

Specifically, the '474 patent fails to disclose, teach, or suggest Applicant's claimed "***providing said instruction reordering mechanism*** having a plurality of said instructions, ***each said instruction port having a respective self-timed vector logic element for causing and preventing launching***, when appropriate, of said instruction." Specifically, the '474 patent fails to disclose, teach, or suggest, "each said instruction port having a respective self-timed vector logic element." The circuits illustrated and described in the '474 patent use clock signals for controlling the propagation of operand dependency logic. Accordingly, for at least this reason, Applicant's independent claim 1 is allowable.

In addition, because the '474 patent fails to disclose, teach, or suggest Applicant's claimed "***providing said instruction reordering mechanism*** having a plurality of said instructions, ***each said instruction port having a respective self-timed vector logic element for causing and preventing launching***, when appropriate, of said instruction;" the '474 patent cannot disclose, teach, or suggest Applicant's claimed "propagating a set of signals successively during a launch cycle ***through said self-timed vector logic elements*** of said instruction reordering mechanism." For at least this additional reason, Applicant's independent claim 1 is allowable.

Because independent claim 1 is allowable, dependent claims 2-9 which depend either directly or indirectly from claim 1 are also allowable. *See In re Fine*, 837, F.2d 1071, 5 U.S.P.Q.2d 1596, 1598 (Fed. Cir. 1988). Accordingly, Applicant respectfully requests that the rejection of claims 1-9 be withdrawn.

2. Claims 10-12

Applicant respectfully traverses the rejection of claims 10-12 under 35 U.S.C. §102(b) for at least the reason that the cited reference fails to disclose, teach, or suggest each element in the claims.

For convenience of analysis, Applicant's independent claim 10, as amended, is repeated below in its entirety.

> 10. A method for quickly finding a predefined plurality of instructions, if available, that are ready to be executed and that reside in a queue of a processor that can launch the execution of instructions out of order, so that the found instructions can be communicated to a corresponding predefined plurality of ports associated with one or more execution resources, comprising the steps of:

(a) providing said queue having a plurality of slots, each said slot for temporarily storing a respective instruction and launching, when appropriate, execution of said respective instruction; and
(b) ***propagating a set of signals successively through slots of said queue during a launch cycle*** that, when passed through a particular slot:
(1) selects said particular slot for launching when said particular slot is ready by asserting in said slot one or more found signals that identify one or more specific ports associated with said one or more execution resources;
(2) refrains from selecting said particular slot when said particular slot is not ready by asserting in said slot a lost signal;
(3) keeps track of how many slots have been selected during said launch cycle; and
(4) causes selection of no more than said predefined plurality of said instructions during said launch cycle; and
wherein propagating occurs in response to logic transitions in only one direction.

(Applicant's independent claim 10 - *emphasis added.*)

Applicant respectfully asserts that the cited art of record fails to disclose, teach, or suggest at least the emphasized step of pending method claim 10 as shown above. Consequently, claim 10 is allowable.

Specifically, the '474 patent fails to disclose, teach, or suggest Applicant's claimed step of "***propagating a set of signals successively through slots of said queue during a launch cycle, . . . wherein propagating occurs in response to logic transitions in only one direction.***" In this regard, the '474 patent apparently describes circuit embodiments responsive to clock signals. That is, clock signals direct the propagation of operand dependency logic. Consequently, the '474 patent does not disclose, teach, or suggest the emphasized step of independent claim 10. Accordingly, for at least this reason, Applicant's independent claim 10 is allowable.

Because independent claim 10 is allowable, dependent claims 11 and 12, which depend from claim 10 are also allowable. *See In re Fine, supra.* Accordingly, Applicant respectfully requests that the rejection of claims 10-12 be withdrawn.

3. Claims 13-22

Applicant respectfully traverses the rejection of claims 13-22 under 35 U.S.C. §102(b) for at least the reason that the cited reference fails to disclose, teach, or suggest each element in the claims.

For convenience of analysis, Applicant's independent claim 13, as amended, is repeated below in its entirety.

> 13. A system for finding a predefined plurality of instructions, if available, that are ready to be executed in a processor that can launch execution of instructions out of order, comprising:
>
> (a) an instruction reordering mechanism for temporarily storing a plurality of said instructions; and
>
> (b) ***a plurality of self-timed vector logic elements associated with said instruction reordering mechanism*** and associated respectively with each of said instructions in said instruction reordering mechanism for causing and preventing launching, when appropriate, of respective instructions, ***said self-timed vector logic elements configured to propagate a plurality of signals through said self-timed vector logic elements such that said self-timed vector logic elements select said predefined plurality of said instructions for launching and de-select any remaining instructions in response to only one direction of logic transition.***

(Applicant's independent claim 13 - *emphasis added.*)

Applicant respectfully asserts that the cited art of record fails to disclose, teach, or suggest at least the emphasized element and limitations of pending claim 13 as shown above. Consequently, claim 13 is allowable.

Specifically, the '474 patent fails to disclose, teach, or suggest Applicant's claimed "***a plurality of self-timed vector logic elements associated with said instruction reordering mechanism . . . said self-timed vector logic elements configured to propagate a plurality of signals through said self-timed vector logic elements such that said self-timed vector logic elements select said predefined plurality of said instructions for launching and de-select any remaining instructions in response to only one direction of logic transition.***" Accordingly, for at least this reason, Applicant's independent claim 13 is allowable.

As described above, the circuits apparently disclosed in the '474 patent do not describe "self-timed vector logic elements," wherein "***said self-timed vector logic elements select said predefined plurality of said instructions for launching and de-select any remaining instructions in response to only one direction of logic transition***." Consequently, the '474 patent cannot anticipate the Applicant's claimed system.

Because independent claim 13 is allowable, dependent claims 14-22, which depend either directly or indirectly from claim 13 are also allowable. *See In re Fine, supra.* Accordingly, Applicant respectfully requests that the rejection of claims 13-22 be withdrawn.

4. Claim 23

Applicant respectfully traverses the rejection of claim 23 under 35 U.S.C. §102(b) for at least the reason that the cited reference fails to disclose, teach, or suggest each element in the claim.

For convenience of analysis, Applicant's independent claim 23, as amended, is repeated below in its entirety.

> 23. A system for finding a predefined plurality of instructions, if available, that are ready to be executed and that reside in a queue of a processor that can launch execution of instructions out of order, comprising:
>
> (a) queue means for storing a plurality of said instructions, said queue means having a plurality of launch logic means for causing and preventing launching, when appropriate, of a respective instruction; and
>
> (b) ***logic means associated with said queue, said logic means for propagating a set of signals to successive launch logic means to indicate both when and which of one or more ports of one or more execution resources are available for each said instruction and when none of said ports are available, wherein said means for propagating is responsive to logic transitions in only one direction.***

(Applicant's independent claim 23 - *emphasis added.*)

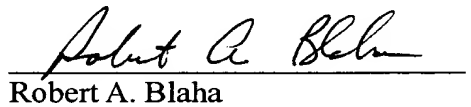
Applicant respectfully asserts that the cited art of record fails to disclose, teach, or suggest at least the emphasized element of pending claim 23 as shown above. Consequently, claim 23 is allowable.

Specifically, the '474 patent fails to disclose, teach, or suggest Applicant's claimed "***logic means associated with said queue, said logic means for propagating a set of signals to successive launch logic means to indicate both when and which of one or more ports of one or more execution resources are available for each said instruction and when none of said ports are available, wherein said means for propagating is responsive to logic transitions in only one direction***." The circuits apparently disclosed in the '474 patent do not describe "***means for propagating a set of signals to successive launch logic means . . wherein said means for propagating is responsive to logic transitions in only one direction***." Consequently, the '474 patent cannot anticipate the Applicant's claimed system. Accordingly, for at least this reason, Applicant's independent claim 23 is allowable. Accordingly, Applicant respectfully requests that the rejection of claim 23 be withdrawn.

CONCLUSION

In summary, Applicant respectfully requests that the outstanding objection of claims 3, 13-23 and the rejection of claims 1-23 be withdrawn. Applicant respectfully submits that presently pending claims 1-23 are allowable and the present application is in condition for allowance. Accordingly, a Notice of Allowance is respectfully solicited. Should the Examiner have any comments regarding the Applicant's response, Applicant requests that the Examiner telephone Applicant's undersigned attorney.

Respectfully submitted,
THOMAS, KAYDEN, HORSTEMEYER & RISLEY, L.L.P.

By: 
Robert A. Blaha
Registration No. 43,502

THOMAS, KAYDEN, HORSTEMEYER & RISLEY, L.L.P.
100 Galleria Parkway, Suite 1750
Atlanta, Georgia 30339-5948
(770) 933-9500